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IN-SITU REMOVAL OF SURFACE IMPURITIES PRIOR TO ARSENIC-DOPED POLYSILICON DEPOSITION IN THE FABRICATION OF A HETEROJUNCTION BIPOLAR TRANSISTOR

[0001] This application claims the benefit of provisional patent application Serial No. 60/426,842 filed on November 15, 2002.

FIELD OF THE INVENTION

[0002] The present invention relates generally to the fabrication of heterojunction bipolar transistors, and more specifically to the removal of certain surface impurities formed during a fabrication process.

BACKGROUND OF THE INVENTION

[0003] Heterojunction bipolar transistors (HBT's) are now widely used in applications where high switching speeds and high frequency operation are desired. The emitter in an HBT has a wider band gap than the band gap of the base, thus creating an energy barrier in the valence band at the emitter-base junction that inhibits the unwanted flow of holes from the base region to the emitter region. Since there is substantially no injection of minority carriers from the base into the emitter, the base impurity concentration can be increased, while maintaining the emitter injection efficiency at a relatively high level. Therefore, it is possible to narrow the base width and lower the internal base resistance, improving the current gain, the emitter injection efficiency and operating cut-off frequency of the transistor, as compared with a conventional bipolar transistor. Progress in epitaxial growth technology of compound semiconductors has fueled the development of HBT's.

[0004] Figure 1 illustrates an HBT 10. A silicon-germanium (SiGe) layer 12 overlies a silicon substrate 14 between two silicon dioxide spacers 16. In stacked relation, the SiGe layer 12 comprises a collector, base, and emitter. A base polysilicon layer 18 forms a contact with the base region 19 of the SiGe layer 12 and is further connected to a base contact, not shown in Figure 1, for accessing the base

region. A silicon nitride layer 22A, silicon nitride spacers 22B, silicon nitride spacers 24 and silicon dioxide spacers 26 separate an arsenic-doped polysilicon layer 30 from the base polysilicon layer 18. A buried doped layer (not shown in Figure 1) within the silicon substrate 14 contacts the collector region, which is disposed at the bottom of the SiGe layer 12, and further is connected to a contact for providing access to the collector.

[0005] The process for forming the HBT 10 is illustrated beginning in Figure 2, showing a stack 38 comprising an silicon dioxide layer 40 (formed preferably by a TEOS (tetraethyl orthosilicate) process), a base polysilicon layer 42, a silicon-nitride layer 44 and an silicon dioxide cap layer 46. The base polysilicon layer 42 is doped p-type prior to formation of the silicon-nitride layer 44.

[0006] In the next process step as illustrated in Figure 3, a window 50 is etched in the stack 38, stopping on an upper surface 54 of the silicon dioxide layer 40. Conventional photolithographic patterning and masking steps, followed by an etch process, are used to form the window 50. As a result of this etching process, the base polysilicon layer 18 and the silicon nitride layer 22A of Figure 1 are formed on opposing sides of the window 50.

[0007] A silicon-nitride layer 58 is formed (see Figure 4) on the field region 59 and within the window 50. After etching, only the spacers 22B remain. See Figure 5.

[0008] Next an emitter window 66 is formed by etching a region of the silicon dioxide layer 40, as illustrated in Figure 6, forming the silicon dioxide spacers 16 on opposing sides of the emitter window 66. Regions 67 of the emitter window 66 undercuts the base polysilicon layer 42 as shown.

[0009] The SiGe layer 12 is then formed epitaxially on the silicon substrate 14. Preferably the SiGe layer 12 comprises in stacked relation from the bottom, a spacer layer, a graded base region (where the Ge doping concentration is graded from the doping in the spacer layer down to about zero) and a silicon cap layer. Boron is introduced into the chamber atmosphere during formation of the base region and the silicon cap layer to form the p-type base. The collector region is formed within the spacer layer by the diffusion of phosphorous from the silicon substrate 14 upwardly into the spacer region of the SiGe layer 12.

[0010] A TEOS oxide deposition forms a silicon dioxide layer 70 followed by the deposition of a silicon-nitride layer 72 as depicted in Figure 8. Both the silicon dioxide layer 70 and the silicon-nitride layer 72 are etched to form the silicon dioxide spacers 26 and the silicon nitride spacers 24 as illustrated in Figure 9.

[0011] According to the prior art, the process continues with a plasma cleaning step in an oxygen and nitrogen atmosphere, followed by a wet or solvent clean. Both steps are intended to remove impurities on a surface 80 of the SiGe layer 12 prior to formation of the arsenic-doped polysilicon layer 30 illustrated in Figure 1. Immediately prior to deposition of the layer 30, the wafer undergoes a pre-clean step in which it is subjected to an HF atmosphere, an HF dip, an RCA clean (a two-step clean using hydrogen peroxide in both steps), and an in situ HF dip and isopropyl alcohol dry. The final in situ HF dip and isopropyl alcohol dry removes any chemical oxides grown during the RCA clean step and forms a hydrogen terminated silicon surface. A hydrogen terminated silicon surface is known to resist native oxide formation in a normal atmosphere at room temperature, presenting a relatively clean surface 80 for execution of the next process step.

[0012] The arsenic-doped polysilicon layer 30 is deposited over the Figure 9 structure to substantially complete formation of the HBT 10 as illustrated in Figure 1. The arsenic-doped polysilicon layer 30 undergoes solid phase epitaxial growth after subsequent thermal processing. Arsenic is diffused from the arsenic-doped polysilicon layer 30 to form the emitter within the SiGe layer 12.

[0013] In certain fabrication processes, formation of the arsenic-doped polysilicon layer 30 is performed in a lamp-based deposition tool wherein the tool chamber is heated to about 700°C by radiant energy prior to and during the deposition process while maintaining a hydrogen flow through the tool chamber. The hydrogen flow maintains the surface 80 in a relatively clean condition during the deposition.

[0014] It is known that other tools can be used to deposit the arsenic-doped polysilicon layer 30, including a hot plate tool wherein the wafer is heated through physical contact with a resistively heated chuck. The hot-plate tool offers certain advantages relative to the lamp-based process for depositing the layer 30, including a more uniform material deposition (thus improving the electrical properties of the final device) and higher wafer through-put. The hot-plate process is performed at about

700°C with a nitrogen flow through the tool chamber both before and during deposition of the arsenic-doped polysilicon layer 30 on the surface 80. It is known that a silicon surface can loose the hydrogen termination condition upon heating. Therefore, the surface 80 is likely contaminated with impurities from the hot plate deposition system or impurities present in the nitrogen gas flow during a temperature stabilization step performed at about 700°C while maintaining a nitrogen flow, before initiating formation of the arsenic-doped polysilicon layer 30.

[0015] It has been determined that fabrication of the layer 30 using the hot plate tool as described above, causes unwanted surface impurities on the surface 80. The observed impurities include oxygen, carbon and nitrogen. It is desired to remove these impurities prior to formation of the arsenic-doped polysilicon layer 30, as they disadvantageously increase the emitter resistance. The impurities also degrade the purity and modify the grain structure of the layer 30 during the subsequent solid phase epitaxial growth, contributing to an increase in the emitter resistance. The impurities can also affect the arsenic diffusion profile in the silicon cap layer.

[0016] One known technique for removing these impurities includes a hydrogen bake, i.e., subjecting the wafer to high temperature hydrogen environment. However, an in-situ high temperature hydrogen bake is impractical while using the hot plate system. The maximum operating temperature for the hot plate system is 800°C. Because the hot plate has high the thermal mass, the thermal recovery time from 800°C to 700°C (the temperature stabilization step) is very long (i.e., greater than fifteen minutes). Although the hydrogen bake process tends to remove some of the impurities, further improvements are warranted.

SUMMARY OF THE INVENTION

[0017] The present invention describes a process for removing contaminants from a surface during fabrication of a semiconductor device of an integrated circuit. The process comprises cleaning the surface, forming a hydrogen termination on the surface, and cleaning the surface with a nitrogen-containing gas at a relatively low temperature.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] The foregoing and other features of the invention will be apparent from the following more particular description of the invention, as illustrated in the accompanying drawings, in which like reference characters refer to the same parts throughout the different figures. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention.

[0019] Figure 1 is a cross-sectional view of an HBT to which the teachings of the present invention can be applied.

[0020] Figures 2 – 9 illustrate the fabrication steps for forming the HBT of Figure 1.

[0021] Figures 10 – 15 depict process steps according to the teachings of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0022] Before describing in detail the particular process for removing surface impurities during fabrication of the arsenic doped polysilicon emitter in an HBT, in accordance with the teachings of the present invention, it should be observed that the present invention resides primarily in a novel combination of method steps. Accordingly, the process steps have been represented by conventional elements in the drawings, showing only those specific details that are pertinent to the present invention, so as not to obscure the disclosure with structural details that will be readily apparent to those skilled in the art having the benefit of the description herein.

[0023] The present invention relates to the use of an in-situ cleaning method to reduce the level of contamination (especially carbon and oxygen contaminants) on a silicon surface prior to the subsequent deposition of doped (e.g., with arsenic, boron, phosphorous or another dopant) or un-doped polycrystalline silicon layer on a doped or un-doped silicon substrate (i.e., bulk silicon or epitaxial silicon).

[0024] One application for use of the present invention is prior to deposition of an arsenic-doped polycrystalline silicon layer, which serves as the emitter contact polysilicon in a silicon germanium (SiGe) graded base NPN bipolar transistor. The SiGe epitaxial structure can be grown by a selective epitaxy process or by a non-selective process. In the SiGe process the germanium concentration is graded from a

high level on the collector side of the base to a low level on the emitter side of the base. In one embodiment of a process for forming the SiGe graded base transistor, the selective SiGe epitaxial structure comprises a SiGe spacer layer (un-doped), a SiGe graded base layer (in one embodiment boron doped), and a silicon cap layer (boron doped in one embodiment). The NPN transistor is formed by subsequent arsenic diffusion from the arsenic-doped polycrystalline layer through the silicon cap layer into the SiGe graded base layer. The collector is formed by phosphorous diffusion from an underling substrate through the SiGe spacer layer into the SiGe graded base.

[0025] Another exemplary application is prior to deposition of an arsenic-doped polycrystalline silicon layer, which serves as the emitter contact in a silicon germanium (SiGe) true heterojunction (HBT) NPN bipolar transistor. As with the graded base NPN bipolar transistor, the SiGe HBT epitaxial structure can be grown by a selective epitaxy process or by a non-selective process. In the SiGe HBT transistor the germanium concentration is high and nominally uniform across the base layer. In one embodiment, the selective SiGe HBT epitaxial structure comprises an upper SiGe spacer layer (un-doped), a SiGe base layer (boron doped in one embodiment), a lower SiGe spacer layer (un-doped) and the arsenic-doped silicon emitter layer. The NPN transistor is formed by subsequent arsenic diffusion from the arsenic-doped emitter layer into the upper SiGe spacer layer, boron diffusion from the SiGe base layer into both the upper and the lower SiGe spacer layers, and phosphorous diffusion from a substrate into the lower SiGe spacer layer. Arsenic also diffuses from the arsenic-doped polycrystalline layer into the arsenic-doped silicon emitter layer, reducing the emitter resistance.

[0026] The present invention teaches several variants of cleaning processes for removal of the impurities on the surface 80 prior to deposition of the arsenic-doped polysilicon layer 30. Certain of the embodiments comprise a cleaning step with NF3 (nitrogen fluoride) at different flow rates, and certain embodiments further comprise a hydrogen bake step. Advantageously, the NF3 clean and the hydrogen bake steps can be performed within the same chamber where the arsenic-doped polysilicon layer 30 is deposited, at about the same pressure as the deposition process and within a

temperature range of the deposition temperature. Thus the process of the present invention is referred to as in-situ clean process.

[0027] In a first embodiment illustrated in Figure 10, the device undergoes a pre-clean step 100, including an HF dip, an RCA clean (a two-step clean using hydrogen peroxide in both steps), and an in-situ HF dip and isopropyl alcohol dry to remove any chemical oxides grown during the RCA clean step and to form a hydrogen terminated surface on the surface 80.

[0028] At a step 102 the device is subjected to an NF3 clean step at a temperature of between about 500° C and about 800°C (a temperature of about 700°C is preferred) for a duration of between about 20 and 80 seconds at a flow rate of about 75 sccm. A preferred duration is about 20 seconds. The pressure during the NF3 clean step is about 275 Torr.

[0029] The arsenic-doped polysilicon layer 30 is then deposited at a temperature of about 700°C and a pressure of about 275 Torr, as depicted by a step 104.

[0030] In the embodiment of Figure 11, a hydrogen bake step 106 is added between the NF3 clean step 102 and the deposition step 104. Hydrogen is supplied to the processing chamber for about 60 to 90 seconds at about 700°C. Although the NF3 removes carbon and oxides from the surface 80, it may leave behind a fluorine contaminant. The hydrogen bake step substantially removes any fluorine.

[0031] In the Figure 12 embodiment, the pre-clean process is separated into individual constituent steps, i.e., the HF dip at a step 112 and the RCA clean at a step 114. The NF3 clean at the step 102 removes chemical oxides deposited on the surface 80 during the RCA cleaning step, and thus the in-situ HF dip step and isopropyl alcohol dry step referred to in conjunction with Figure 10 are not necessary. Following the NF3 clean step 102, the arsenic-doped polysilicon layer 30 is deposited at the step 104.

[0032] The Figure 13 embodiment is similar to the Figure 12 embodiment, and includes the hydrogen bake step 106 immediately preceding deposition of the arsenic-doped polysilicon layer 30.

[0033] In the embodiments represented by the Figure 14 and 15 process flowcharts, the pre-clean step 100 included in previous embodiments is replaced by an NF3 process 120 that serves to both clean the surface 80 and etch oxides, carbon and

nitrogen that have formed there during previous process steps. This NF3 process is conducted at a flow rate of about 200 sccm. The Figure 15 embodiment includes the hydrogen bake step 106 between the NF3 process 120 and deposition of the arsenic-doped polysilicon layer 30 at the step 104.

[0034] The various embodiments of the present invention can be practiced with the formation of the in situ arsenic-doped polysilicon layer 30 as described herein, and with a process employing implant doping after depositing an un-doped polysilicon layer.

[0035] Although explained with reference to the deposition of a polysilicon doped emitter region of an HBT, the teachings of the present invention can be applied more generally to the deposition of doped and un-doped polysilicon over a doped or un-doped epitaxially grown layer or a doped or un-doped bulk silicon substrate. For example, the method according to the teachings of the present invention can be employed to clean an epitaxial or bulk silicon surface prior to the deposition of doped or un-doped polycrystalline silicon in a contact window to form a polysilicon contact with the epitaxial or bulk silicon.

[0036] While the invention has been described with reference to preferred embodiments, it will be understood by those skilled in the art that various changes may be made and equivalent elements may be substituted for elements thereof without departing from the scope of the present invention. The scope of the present invention further includes any combination of the elements from the various embodiments set forth herein. In addition, modifications may be made to adapt a particular situation to the teachings of the present invention without departing from its essential scope thereof. Therefore, it is intended that the invention not be limited to the particular embodiment disclosed as the best mode contemplated for carrying out this invention, but that the invention will include all embodiments falling within the scope of the appended claims.